Reference Jitter Cleaning DPLL Without Oscillator-Generated Output Noise Suffering

Granite SemiCom has developed a fourth generation Digital Phase-Locked Loop intended for “jitter-cleaning” applications where the input reference may be at very low frequencies, and can have excessive jitter, as high as 5% of its period (or higher depending on the specification for the output jitter). The design of Phase-Locked Loops for this application historically involves a compromise between minizing jitter due the noisy input and minimizing jitter due to the oscillator. To minimize jitter due to the input reference, one would normally choose a low cut-off frequency for the loop bandwidth; to minimize jitter due to the oscillator, one would normally design the PLL to have a high bandwidth. GSC has developed a new architecture which circumvents this compromise by having two independent transfer functions; a high bandwidth from the oscillator jitter to the output, and a very low bandwidth between the reference input and the output.

The relationship between input phase jitter and output jitter of a PLL is modeled assuming a linear transfer function (linearized about the PLL's operating point after convergence). The great majority of PLL's can be modelled in the continuous-time domain using an input to output function of the form:

$$H_{CL}(s)=\frac{s+\omega_z}{\frac{s^2}{\omega_z\omega_P}+\frac{s}{\omega_z}+1} \tag{1}$$

The constant ω_z determines the gain of the feedforward integral path of the PLL. In an analog PLL, this is determined by the size of the capacitor in the PLL loop filter, and the magnitudes of the charge-pump current sources that charge the same. Most current PLL's are over-damped, or equivalently have a Q-factor quite a bit less than $1/\sqrt{(2)}\simeq 0.7071$. The Q-factor of the denominator of (1) is given by.

$$Q=\omega_z/\omega_p \tag{2}$$

For $Q\ll 0.7071$, the PLL closed-loop bandwidth is given by:

$$\omega_{-3\,dB}\simeq\omega_P \tag{3}$$

This PLL loop-bandwidth is perhaps the most important parameter to choose when designing a PLL; it has significant effects on the output jitter. For classical PLL's, it's choice is a compromise between minimizing output jitter due to input jitter as opposed to minimizing output jitter due to the oscillator-jitter and power-supply-noise. To minimize output jitter caused by jitter in the input reference, the PLL closed-loop bandwidth should be chosen low. To minimize jitter caused by the oscillator due to power-supply noise, thermal noise, and especially 1/f noise, the loop bandwidth should be chosen high. This trade-off is fundamental in classic architectures.

The new DPLL uses two references, one from a clean crystal reference source, that might be between 100-200MHz, with the oscillator running at 5GHz. This is a common situation for realizing high-quality low-jitter output clocks. This DPLL has advanced fractional division capability (Frac/N), so non-integer relationships between the 100-200MHz reference, and the PLL output clock can be

achieved with high resolution. This DPLL is digital in that it does not have analog charge-pumps; these are hard to realize in sub-micron technologies due to issues such as leakage current in the capacitors used in the loop filters, excessive reference feedthrough due to offsets, low voltage head-room necessitating large gain (and therefore noise gain), the need for voltage regulation to minimize jitter caused by power-supply noise, etc. In GSC's DPLL, the loop filters are digital, scale with the reference frequency, and their performance is accurately predicted using fast verilog simulations, with few second-order, technology-dependent effects.

Granite SemiCom has extended its DPLL for jitter cleaning applications, where the reference input may be at very low frequencies, and might have excessive jitter. The loop bandwidth for the second reference (as opposed to the higher-frequency reference input), can be chosen independently from the bandwidth of the DPLL locked to the high-frequency crystal reference. For example, with the second reference at 10MHz, a loop bandwidth as low as 3kHz can be chosen, whereas the the bandwidth for the crystal reference might be chosen to be between 3 and 5 MHz. This relatively high-loop bandwidth minimizes output jitter caused by the oscillator. The much lower bandwidth filtering the jitter of the second input reference, does not negatively effect the output jitter due to the oscillator. There is also a second Frac/N so the relationship between the oscillator and the second reference input can also be arbitrarily chosen. The extensions for this jitter-cleaning application are all digital, and practically all at low frequencies. They do take some additional area, but not much in sub-micron technologies. The increase in power dissipation is negligible as the digital circuits are mostly operating at low clock rates. Also, because the extensions are completley digital, they are accurately simulated using verilog which is accurate to the bit-level and used to verify excellent stablility and settling. Basically, what you simulate is what you get and risk is greatly minimized. The advantages of this extended architecture over the previous excellent DPLL are significant for jitter-cleaning applications with low-frequency reference inputs.