High-Speed Digital PLL (HSDPLL)

Granite SemiCom Inc.

High-Speed, Wide-Range Digital Clock-Driver and Clock-Multiplying Unit

Granite Semicom has recently tested first silicon of its totally-integrated (no off-chip components) Clock-Driver and Clock-Multiplying-Unit IP block with fractional-N division to allow for non-integer clock multiplication and spreading. This block is intended for applications such as the CMU in a SERDES block at data rates as high as 15 Gbs (and potentially higher), and for clock-driver applications where the frequencies are not integrally related. This IP block is a digital phased-lock-loop, plus an integrated voltage and current reference, a variety of input amplifiers (single-ended and differential, dc and ac-coupled), a number of programmable dividers, a serial interface for programming, and a high-speed 50 ohm driver capable of driving off-chip at full-speed. The specification is for the High-Speed Digital PLL (HSDPLL) to operate between 0.5GHz and 7.5GHz over process corners and between -40 and 125 degrees celsius; the first measured sample locks for output frequencies between 0.144GHz and 10.8GHz, dissipates 32 mw (at a 5GHz output), and requires a 0.11 mm^2 area (not including pads and the output driver). Jitter measurements are on-going, but first off-chip measurements (after the output driver and 2cm of PCB trace) indicate total rms accumulated jitter of 1.6ps a 5GHz output frequency.

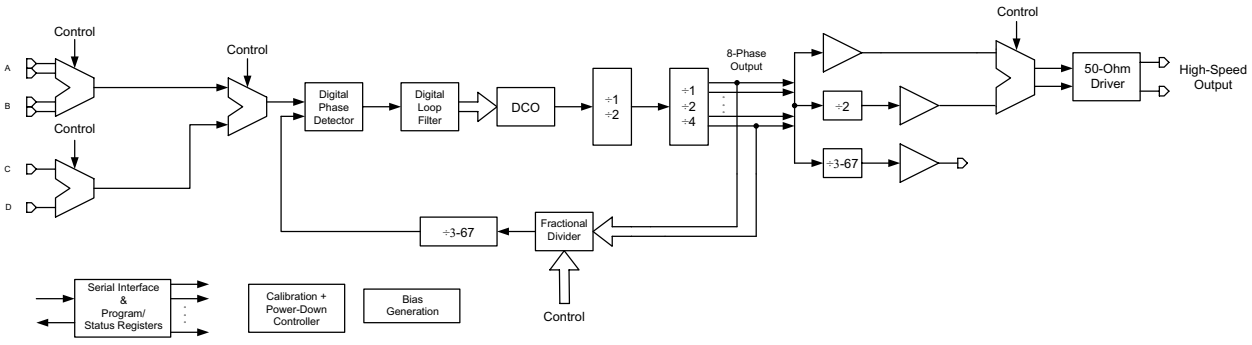

Fig. 1. Block diagram of HSFDPLL-V100 digital PLL and clock-driver IP.

What is a Digital PLL?

Practically all modern PLL's are actually mixed-mode analog/digital blocks; what is commonly meant by a *Digital PLL* is a PLL that is mostly digital, that does not have an analog loop

filter, and that also does not have analog charge-pump circuits. These sub-components are replaced with digital equivalents in a ***Digital PLL.***

Why a Digital PLL?

1. **Wide Range and Programmability:** A digital PLL is much easier to design to be used over a wide range of reference frequencies and output frequencies. The main reason for this is the dynamics of the integral signal path automatically track with the reference frequency. This should be compared with an analog approach where the analog loop filter must be *'digitally trimmed'* for different bandwidths and reference frequencies, and the tuning range is limited. In addition, a highly-programmable digital approach can be digitally adjusted for many different application requirements; this allows for a ***One Size Fits All,*** minimizing both costs and support complexities. The programmability includes output impedance, loop bandwidth, output division ratio, VCO load capacitance, input reference amplifier type, etc.
2. **Predictability:** the PLL is primarily composed of digital logic circuits which are highly predictable especially in sub-micron processes. ***What you simulate is what you get.*** Digital circuits are not affected (to the same degree) by analog issues such as leakage currents through loop capacitors, offset voltages due to transistor mismatches, substrate noise, reference feedthrough, etc (effects minimized, not eliminated). Predictability is critical as one goes to 40nm and smaller technologies; a second iteration caused by a poorly working PLL can incur millions of dollars of costs and loss of revenue and months lost in time to market.
3. **Porting:** porting a PLL to a new technology is much faster and involves much less risk for a Digital PLL; for example, two silicon fabrication iterations, as required to center an LC oscillator, are not necessary. The GSC Digital PLL was designed using a technology independent approach, and practically all parameters (including loop transfer-function parameters) accurately scale proportional to the oscillation frequency. The bias circuits are all done in the high voltage option, and their absolute sizes accommodate all popular high-voltage options (1.8V/0.18um, 2.5V/0.25um, and 3.3V/0.35um), the minimum channel lengths accommodate higher voltages, while they can be used with a high-voltage as low as 1.62V and as high as 4V (a 5V high-voltage is also possible with minimal changes). Porting simply involves transferring the digital library (which again has been designed in a technology-independent manner) and modifying the resistors in the bias circuits for the new resistivity. Any process uncertainties are calibrated out at start-up, or adaptively digitally trimmed during circuit operation, without glitches. *Another, strongly related characteristic is customization is much faster, cheaper, and safer, as it generally involves minimal logic changes only.*
4. **Size:** because the loop-filter and analog charge pumps have been eliminated, the size ($0.11 mm^2$ is similar to or smaller as compared to analog approaches; this is especially true as one goes to smaller technologies.
5. **Jitter:** a major source of jitter for analog PLL's (often the dominant source of jitter) comes from the loop filter, charge-pumps, and V/I conversion circuits. This is especially the case when non-calibrated charge-pump offsets, and power-supply noise are considered. These jitter noise sources can be significantly minimized with a properly designed digital approach. Currently, the accumulated rms jitter has been measured (using 1667 golden filter) at 1.6ps for a 5GHz output. The next iteration (planned to tape out Q2/2012) is predicted to measure at less than 1.0ps rms accumulated jitter.

6. **Testing:** the HSDPLL has a number of built-in testing features that can assessed through the SPI bus; these include access to the calibration values to characterize the speed of the process, an "IN-LOCK" output, and a built-in accummulated jitter measurement that gives the highest confidence all it working as expected.

Why Not?

Historically, the digital update, and the digital phase-detector have injected large jitter at each update; digital PLL's have not obtained the jitter performance of analog PLL's. GSC has solved the glitch problem at digital updates, has a significantly superior ring-oscillator, has greatly minimized charge-pump, loop-filter, and V/I conversion noise, etc. Its approach and its jitter performance, for a given power, oscillation and reference frequencies and loop bandwidth, is superior to other ring-oscillator-based approaches, and approaches the jitter performance of many LC-based approaches.

Specifications:

As is the case for all PLL's, the specifications are dependent on the power, oscillation frequency, reference frequency, loop bandwidth, and loop damping factor. All specification numbers are based upon either measurements or careful simulations over process and corners.

An example set of specifications for a loop optimized for high-frequency (a 5GHz oscillation frequency for a 10Gb/s half-rate SERDES application) 100MHz reference frequency, a 3MHz loop bandwidth (with moderate overdamping) and a 1.8V high-voltage option, are:

1. **Power:** measured at 32 mW excluding output driver.
2. **Temperature:** -40° C to 125° C.
3. **Jitter:** accumulated total jitter using a 1667 golden-filter (1.5-2 ps rms depending on bandwidth and reference frequency. The numbers go up about 10-15% with the frac/N turned on. We expect much of this noise is from the pad ring and board, and to improve on it with further measurements. In a second silicon, scheduled to go out in Q2 2012, we expect, with confidence, to get this down to below 1.0 ps accumulated jitter., for a 5Ghz output.
4. **Lock Times**: less than 10 us for complete calibration at start-up and lock (nominally 5-6 us); and less than 1us for lock from power-down when calibration has been remembered from previous power-up. The calibration is a new, fast-adapting approach. In addition, the integral path convergence has advanced gear shifting to allow for both fast adapting while still having a large damping factor (which minimizes loop transfer-function peaking).
5. **Off-Chip Components:** none.
6. **PSRR:** better than 46 dB (voltage to free-running oscillation frequency) at lower frequencies, peaking less than 20 dB at all frequencies across process and temperature.
7. **Fractional/N Capability:** included; this can be removed to save space when not needed. When included, it can be enabled or disabled. When enabled, it increases jitter by 10%-15%.
8. **Temperature Stability:** all process variations are calibrated out at start-up (±50 % capability), the integral path can handle ±12 % whereas the free-running frequency (which is calibrated by the integral path) only varies by less than 5% over -40° C to 125° C (2% for band-

gap, 3% for oscillator). Since all loop parameters are proportional to the free-running frequency, which is calibrated, effectively all loop parameters are accurate to around 1%-2%.

9. **Programmability:** there is a divide-by one or two, followed by a multi-output-phase (8) divide by 1, or 2, or 4 divider right after the oscillator inside the feedback loop followed by a 6-bit programmable feed-back divider. These give a very wide range on the ratio of effective oscillator frequency (the output of the first dividers) to reference frequency (the output of the second divider). In addition, outside the loop at the output, one can take the full-rate output, a half-rate output, or the output from a 6-bit programmable output. The loop bandwidth, damping factor, free-running frequency, Frac/N, and bias currents are all programmable (through an SPI serial interface - this can easily be replaced by an I^2C interface). There are 18 8-bit configuration registers, and 8 8-bit status only registers, for testing and characterization. There is also an analog testing multiplexor (for characterization) whose inputs can be selected. All programming registers have default values, so often programming is not necessary. A Graphic-User-Interlace (GUI) (used in both simulation and design) is available for programming the registers, to guarantee defaults are all set correctly, and to ease the integration into an SOC.