GSC's Digital PLL in TSMC 28nm HPM Process

Granite SemiCom Inc.

DPLL28 Overview

Granite SemiCom Inc. (GSC) has just completed the design, layout, and verification, of it's digitall PLL (DPLL) for realization in TSMC's 28nm HPM process; this is GSC's third DPLL (developed over the previous five years). Fabrication is currently scheduled for the first quarter of 2014. The intended applications are for general purpose, moderately high speed, clock generation applications where small area and power are critical without sacrificing quality. Previous generations (realized in TSMC's 40G and 40LP processes) were intended for the highest speeds possible for a PLL based on a wide-frequency-range ring-oscillator necessitating higher power. The new DPLL28 has traded off speed for greatly minimized power and area, yet retaining excellent jitter for the intended speeds (rms period jitter less than 0.1% of the ouput period). An example application might be for generating a clock in a DDR3 controller or in the CMU for multi-lane chip-to-chip serial links where a large number of CMUs are required. The area of the DPLL, including a completely integrated voltage reference with no off-chip components, is less than 0.06 mm^2. The frequency range of the output signal over PVT is 50kHz to 4 GHz. Power varies with the frequency of the oscillator and the voltage of the I/O power supply, but a typical number for a 3.2GHz oscillator frequency and a 1.5V I/O supply voltage is 7mW (worst case over PVT is 9 mW); this includes the power of the integrated band-gap voltage reference. For a 1.6GHz oscillator frequency, with a 1.2V I/O supply voltage, typical power is less than 4mW. The temperature range is -40° C to 125° C and the acceptable voltage of the I/O supply is 1.2V to 2V.

The DPLL has a number of design features that make general purpose use simple and easy. It has a wide variety of programmable dividers; their division ratios can be determined by defaults at start-up where the defaults are determined by dc connections of pins at the edge of the DPLL (to either a "Tie-High" or a "Tie-Low"). In addition, the DPLL is widely reconfigurable after the fact by programming internal registers through either a serial SPI interface, or optionally a parallel interface (both are included). The registers can be programmed using a supplied Graphical User Interface (GUI) where the required values are determined automatically, and documentation for each register is included. Fractional-division capability is available, and the ouput has a programmable divide-by-one or divide-by-two at the output which can be changed "on-the-fly" without glitches or reduced-width pulses. In most applications, the DPLL can be used "right-out-of-the-box"; however, in specialized applications where customization is necessary, this can be accommodated on a time-and-materials cost flow-through business model. A block diagram of the DPLL28 is shown in Fig. 1.

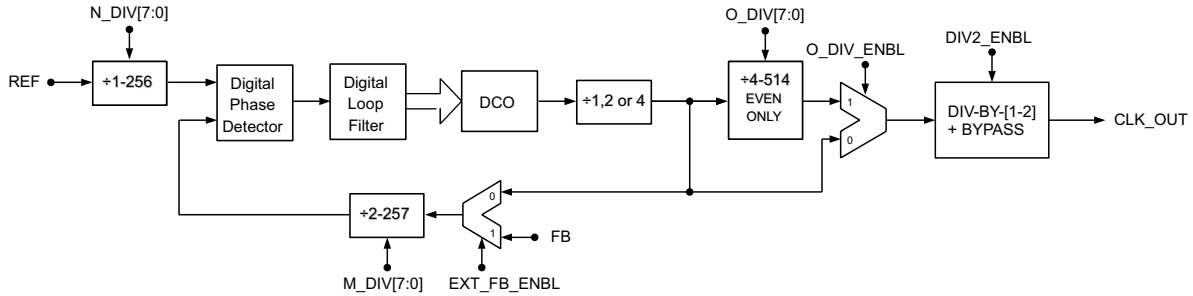

Fig. 1. Block diagram of GSC's DPLL28, designed forTSMC's 28HPM process.